REMARKS

Reconsideration of this application is respectfully requested.

Since claim 11 has now been cancelled without prejudice or disclaimer, the outstanding formal objection to claim 11 has been mooted.

The rejections of all original claims 1-14 under various allegations of anticipation and/or obviousness based on Suzuki '108 (claims 1, 2 and 6) or Suzuki '108 in view of "well established teaching in art" (claims 3 and 8) or Suzuki '108 in view of Susnow '329 (claims 4, 5, 9 and 10) or Suzuki '108 in view of Findlater '138 (claim 7) or Suzuki '108 in view of Satou '327 (claim 11) or Suzuki '108 in view of "well established teaching in art" (claims 12 and 13) or Suzuki '108 and well established teaching in the art and in further view of Susnow '329 (claim 14) are all respectfully traversed.

All of these grounds of rejection are fundamentally based on Suzuki '108. Accordingly, all such rejections fall if Suzuki '108 is demonstrated as being deficient.

While Suzuki '108 may be read broadly to disclose reading and writing out of an elasticity buffer using different clocks with proximity of the reading and writing sequences being used to control insertion/removal of idle bytes or the like to maintain synchronization, this reference in no way teaches (or suggests) the novel and advantageous structure for achieving this overall result now more specifically recited in applicants' claims.

In particular, as now claimed by the applicants, the elastic buffer has at least three but definitely not more than five locations; the monitoring of the reading and writing sequences being done by monitoring the pointers. Re-synchronization as a consequence of the reading clock being too late is achieved when the write pointer points at location (a) and the read pointer points at the very next location (b), and that the read clock is indicated too early when both read and write pointer point at location (a). Proper synchronized operation will occur when the read pointer is pointing to a third location (d), so that the absolute minimum number of locations is three. If one wishes to permit jitter than the minimum number of locations is five, as may be observed from the specification at the top of page 3. Then when the write pointer is pointing to location (a), and read pointer is pointing to location (d) there is effectively synchronism. For the write pointer pointing at location (a), there is tolerable jitter when the read pointer points at location (c) or location (e). When it points at location (b) the read pointer is too late and when the read pointer points at location 9a) the read clock is too early.

Claim 1 has been amended to specify at least three but not more than five locations and the other limitations mentioned above. Similar amendments have been made to claim 6 and claim 12. New claims 15 and 16 indicate the significance of the other phase positions in the special case where there are five locations.

Applicant has amended the claims so as to point out more distinctly the subject-matter of the invention. In particular, claims 1, 6 and 12 have been amended to specify the particular nature of Applicants' slip detector which monitors the state of synchronism

or an elastic buffer. Suzuki employs a FIFO buffer. The James reference shows a comparatively small elasticity buffer (four to eight locations) which however requires the writing in of flag bits to the storage locations and the monitoring of the phase of the signal obtained by reading the flag bits.

In the applicants' slip detector, the detection of a read clock which is too late is determined when the read pointer points to the very next storage locations e.g. (b) in the cyclic sequence after the storage location e.g. (a) which is indicated by the write pointer. The state of a too early read clock is denoted when the read and write pointers are pointing to the same location, e.g. (a). There has to be a minimum of three storage locations since one is required to denote synchronism of the clocks and not occasion or indicate any resynchronization. thus the size of the buffer is not arbitrary and the Applicants' particular definition of a too early and too late clock is the key to providing a buffer of absolutely minimum size (three locations). Likewise, as specified more particularly in claims 15 and 16, the introduction of two further storage locations, giving a maximum of five storage locations, is the key to providing a buffer which is of minimum size yet will tolerate two-way jitter between the write and read clocks.

None of the prior art discloses or suggests the particular form of monitoring to determine wheat constitutes a read clock which is too early and too late relative to the write clock. In particular, there is no suggestion in the art that the too late clock should be indicated when the write and read pointers are pointing at immediately adjacent

locations and that a read clock which is too early is indicated when the read and write pointers are pointing to the same location.

The Examiner's attention is also drawn to new method claims 17-19 which may be analogized to apparatus claims 1, 2 and 15. These method claims are believed to be allowable for reasons similar to those already discussed with respect to corresponding apparatus claims.

Accordingly, this entire application is now believed to be in allowable condition and a formal notice to that effect is respectfully solicited.

Respectfully submitted,

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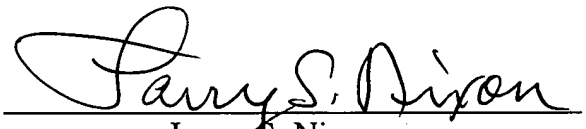
By: 
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